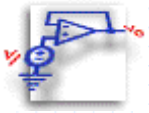

Section 3.1b Review of System Transients

Section 3.1.3 Transient Overvoltages

Transient overvoltages are due to network ringing at the beginning of the transient. Temporary overvoltages are caused at steady state due to reactive power unbalance in the system. Consider the single phase representation of a power system, shown in Figure 3.1.2. For the purpose of studying the two different types of overvoltages, the system in front of the load bus can be represented by a Thevenin source. The load at the bus is represented by a series RL equivalent. The bus capacitor accounts for the line charging variables and for additional compensation to compensate for the load reactance.

Although in a practical problem a more complex system representation is required, the single phase example below demonstrates the conditions under which transient and temporary overvoltages manifest and their main characteristics.

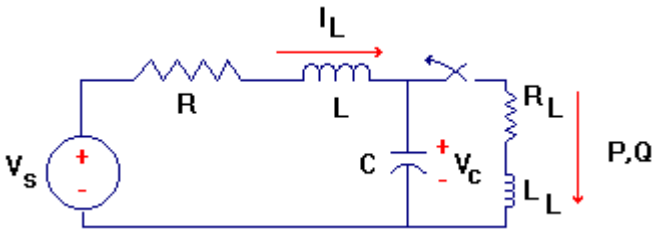

Fig. 3.1.2 Load rejection

Consider the following system parameters,

$L := 0.050\ H$ $R := 5.0\ \Omega$ $C := 0.000013\ F$

$P := 200\ W$ $\phi := 30\ deg$

$V_s(t) := \sqrt{2} \cdot 200 \cdot \cos(\omega \cdot t + \phi_s)\ V$ with $\omega \equiv 377\ \frac{rad}{s}$

The load equivalent circuit can be found as

$Q := P \cdot \tan(\phi)$ load reactive power

$Q = 115.47\ W$

$Z_L := \frac{(200\ V)^2}{\sqrt{P^2 + Q^2}}$ load impedance

$Z_L = 173.205\ \Omega$

$R_L := Z_L \cdot \cos(\phi)$ $R_L = 150\ \Omega$

$L_L := \frac{Z_L \cdot \sin(\phi)}{\omega}$ $L_L = 0.23\ H$

The system operates at steady state, prior to opening the breaker at t = 0. The system steady state prior to the load rejection is calculated as

$Z_L := R_L + 1\mathrm{j} \cdot \omega \cdot L_L$ load impedance in complex form

$Z1 := \dfrac{1}{1\mathrm{j} \cdot \omega \cdot C + \dfrac{1}{Z_L}}$ combination of capacitor and load impedances

$Zt := R + 1\mathrm{j} \cdot \omega \cdot L + Z1$ total impedance source sees

$V_{ps} := 200 \cdot \boldsymbol{V} \cdot \boldsymbol{e}^{1\mathrm{j} \cdot \phi_s}$ phasor representation of source voltage

Therefore, the line current is

$I_{line} := \dfrac{V_{ps}}{Zt}$ $\left|I_{line}\right| = 1.086\ \boldsymbol{A}$

and the voltage at the load bus is

$V_{load} := V_{ps} \cdot \dfrac{Z1}{Zt}$ $\left|V_{load}\right| = 201.505\ \boldsymbol{V}$

After the opening of the breaker, the equivalent circuit is reduced to that of Figure 3.1.1. The system response can be obtained following similar steps as in the case of a second order circuit. This section demonstrates how a numerical integration method can be used to obtain the system response. With reference to Section 3.1.2, we define the following functions providing the derivatives of the inductor current and capacitor voltage respectively.

$$DI_L(I_L, V_C, t) := \frac{-R \cdot I_L - V_C + V_s(t)}{L} \qquad DV_C(I_L, V_C, t) := \frac{I_L}{C}$$

Define the integration step.

$dt := 0.1\ \boldsymbol{ms}$

Define

$h1 := 1.5 \cdot dt$ $h2 := 0.5 \cdot dt$

Define the duration of the simulation.

$T := 0.09\ \boldsymbol{s}$

The initial conditions can be found from the pre-disturbance steady state.

$I_{L_0} := \sqrt{2} \cdot \left|I_{line}\right| \cdot \cos\left(\arg\left(I_{line}\right)\right)$

$V_{C_0} := \sqrt{2} \cdot \left|V_{load}\right| \cdot \cos\left(\arg\left(V_{load}\right)\right)$

The system transient overvoltage depends on the instant of switching. This time can be adjusted by adjusting the source phase angle. Assume

$\phi_s \equiv 0 \cdot \boldsymbol{deg}$

The system numerical solution is obtained as

$$I_{L_1} := I_{L_0} \qquad V_{C_1} := V_{C_0}$$

$$N := \text{floor}\left(\frac{T}{dt}\right) \qquad t_0 := 0\ s \qquad t_1 := 0\ s$$

$$i := 1 .. N$$

$$\begin{bmatrix} t_{i+1} \\ I_{L_{i+1}} \\ V_{C_{i+1}} \end{bmatrix} := \begin{bmatrix} t_i + dt \\ I_{L_i} + h1 \cdot DI_L\left(I_{L_i}, V_{C_i}, t_i\right) - h2 \cdot DI_L\left(I_{L_{i-1}}, V_{C_{i-1}}, t_{i-1}\right) \\ V_{C_i} + h1 \cdot DV_C\left(I_{L_i}, V_{C_i}, t_i\right) - h2 \cdot DV_C\left(I_{L_{i-1}}, V_{C_{i-1}}, t_{i-1}\right) \end{bmatrix}$$

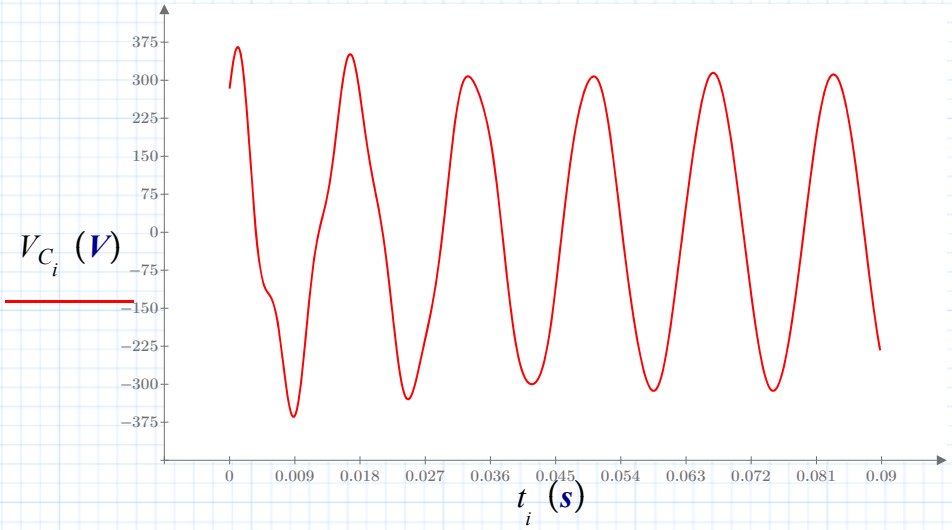

Fig. 3.1.3 System transient and temporary overvoltage

From the above graph it is observed that initially the bus experiences a high overvoltage due to the system ringing. The system ringing is the result of resonance between the bus capacitance and the line inductance. This part of the response decays according to the system damping determined by the line resistance. As the system approaches steady state, the bus experiences a sustained overvoltage that is due to excessive reactive power production by the bus capacitor. This temporary overvoltage increases the requirements for the arrester energy.

Section 3.1.4 Harmonic Overvoltages

Harmonic overvoltages on a bus are sustained overvoltages due to the interaction between the system harmonic impedance as seen from the bus and system devices that may generate harmonics. The system harmonic impedance contains resonances determined by the L and C parameters of the system. If a device injects harmonic current into the bus, the injected frequencies may fall near the resonance frequencies of the system impedance. This interaction produces a sustained resonance which, depending on the system damping at the resonance frequencies, can produce excessive overvoltages.

Conditions that can cause harmonic overvoltages include

(a) Excessive transformer magnetizing current: The transformer magnetizing current is non-sinusoidal and, therefore, it may interact with the system impedance. These interactions are particularly pronounced at low order harmonics where the harmonic content of the magnetizing current is higher. The transformer draws excessive magnetizing current during energization and in overvoltage conditions where transformer saturation is more pronounced.

(b) Power electronic equipment: This type of equipment inherently generates current harmonics due to the switching action of the power converters. The order and amplitude of the current harmonics depend on the type of converter and they are called **characteristic harmonics**. For the normal operation of this equipment, harmonic filters are installed on the system bus to absorb the device characteristic harmonics. However, the converter may produce harmonics of uncharacteristic order. Since filtering is not provided for these orders, interactions may occur between the converter current injections and the system harmonic impedance. Another condition that can produce harmonic interactions is temporary system frequency change, which results in the detuning of the converter harmonic filters.

To learn more about harmonic calculations in power systems, see **Section 1.5a**.

For the purpose of demonstration, consider the scenario of Section 3.2.3. A harmonic current source is injected into the load bus. This source represents the harmonics of the **transformer magnetizing current** immediately following the load rejection.

$$I_T(t) := 0.8\ \boldsymbol{A} \cdot \cos(2 \cdot \omega \cdot t) + 0.4\ \boldsymbol{A} \cdot \cos(3 \cdot \omega \cdot t)$$

The system representation is as in the previous example except that the derivative of the capacitor voltage is now given by

$$DV_C\langle I_L, V_C, t\rangle := \frac{I_L - I_T(t)}{C}$$

The simulation steps are the same as in the previous example.

Define the integration step.

$$dt := 0.1\ \boldsymbol{ms}$$

Define

$$h1 := 1.5 \cdot dt \qquad h2 := 0.5 \cdot dt$$

Define the duration of the simulation.

$$T := 0.09\ s$$

$$N := \text{floor}\left(\frac{T}{dt}\right)$$

$$i := 1 .. N$$

$$\begin{bmatrix} t_{i+1} \\ I_{L_{i+1}} \\ V_{C_{i+1}} \end{bmatrix} := \begin{bmatrix} t_i + dt \\ I_{L_i} + h1 \cdot DI_L\left(I_{L_i}, V_{C_i}, t_i\right) - h2 \cdot DI_L\left(I_{L_{i-1}}, V_{C_{i-1}}, t_{i-1}\right) \\ V_{C_i} + h1 \cdot DV_C\left(I_{L_i}, V_{C_i}, t_i\right) - h2 \cdot DV_C\left(I_{L_{i-1}}, V_{C_{i-1}}, t_{i-1}\right) \end{bmatrix}$$

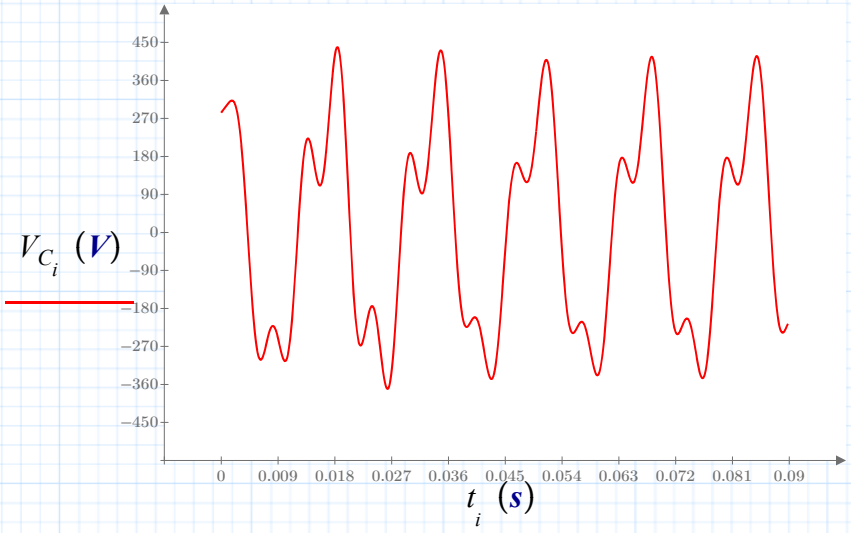

Fig. 3.1.4 Harmonic overvoltage

Section 3.1.5 Breaker Recovery Voltage

Part of the transient phenomena studies includes the study of the recovery voltage appearing across a circuit breaker during opening operation. Excessive recovery voltage may impair the breaker's ability to interrupt the current. Proper circuit representation of the system can provide an estimate of the recovery voltage.

With reference to Figure 3.1.3, the fault occurs at the load side of the breaker. The fault current is essentially limited by the system inductance. As soon as the contacts of the circuit breaker open, an arc will develop which will sustain the fault current. Upon extinction of the arc, the fault current will be interrupted near its natural zero crossing. As soon as the fault current has been interrupted, the capacitance on the other side of the breaker will charge to the source voltage through the system inductance. Due to the resonance in the system, the capacitor voltage and, therefore, the breaker recovery voltage will overshoot reaching its first maximum value. The rate of change of the recovery voltage at the initial system ringing and its maximum value will stress the breaker insulation. The arc may reignite and the fault current may restrike if the breaker has not built sufficient insulation withstand capability at the moment of the recovery.

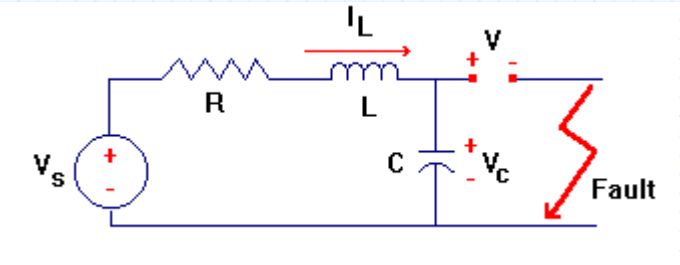

Fig. 3.1.3 Fault current interruption

The analysis of the recovery voltage can commence at the moment of fault current interruption. With respect to the source voltage, this happens at a phase angle equal to the system impedance angle. Consider the following parameters.

$\omega := 377 \ \frac{rad}{s}$ system frequency

System impedance is dependent upon

$L := 0.015 \ H$ $R := 1.0 \ \Omega$ $C := 0.000001 \ F$

$\phi := \operatorname{atan}\left(\frac{\omega \cdot L}{R}\right)$ system impedance angle

$V_s(t) := \sqrt{2} \cdot 200 \ V \cdot \cos(\omega \cdot t - \phi)$

The simulation procedure followed is described in **Section 3.1a**.

$dt := 10 \ s \cdot 10^{-6}$ time step

$T := 5 \ ms$ simulation time

$DI_L(I_L, V_C, t) := \frac{-R \cdot I_L - V_C + V_s(t)}{L}$ $DV_C(I_L, V_C, t) := \frac{I_L}{C}$

Initial conditions:

$I_{L_0} := 0\ A$ interruption at current zero

$V_{C_0} := 0\ V$ capacitor unenergized during fault

$h1 := 1.5 \cdot dt$ $h2 := 0.5 \cdot dt$

$N := \text{floor}\left(\frac{T}{dt}\right)$

$i := 1 .. N$

$I_{L_1} := I_{L_0}$ $V_{C_1} := V_{C_0}$

$t_0 := 0\ s$ $t_1 := 0\ s$

$$\begin{bmatrix} t_{i+1} \\ I_{L_{i+1}} \\ V_{C_{i+1}} \end{bmatrix} := \begin{bmatrix} t_i + dt \\ I_{L_i} + h1 \cdot DI_L\left(I_{L_i}, V_{C_i}, t_i\right) - h2 \cdot DI_L\left(I_{L_{i-1}}, V_{C_{i-1}}, t_{i-1}\right) \\ V_{C_i} + h1 \cdot DV_C\left(I_{L_i}, V_{C_i}, t_i\right) - h2 \cdot DV_C\left(I_{L_{i-1}}, V_{C_{i-1}}, t_{i-1}\right) \end{bmatrix}$$

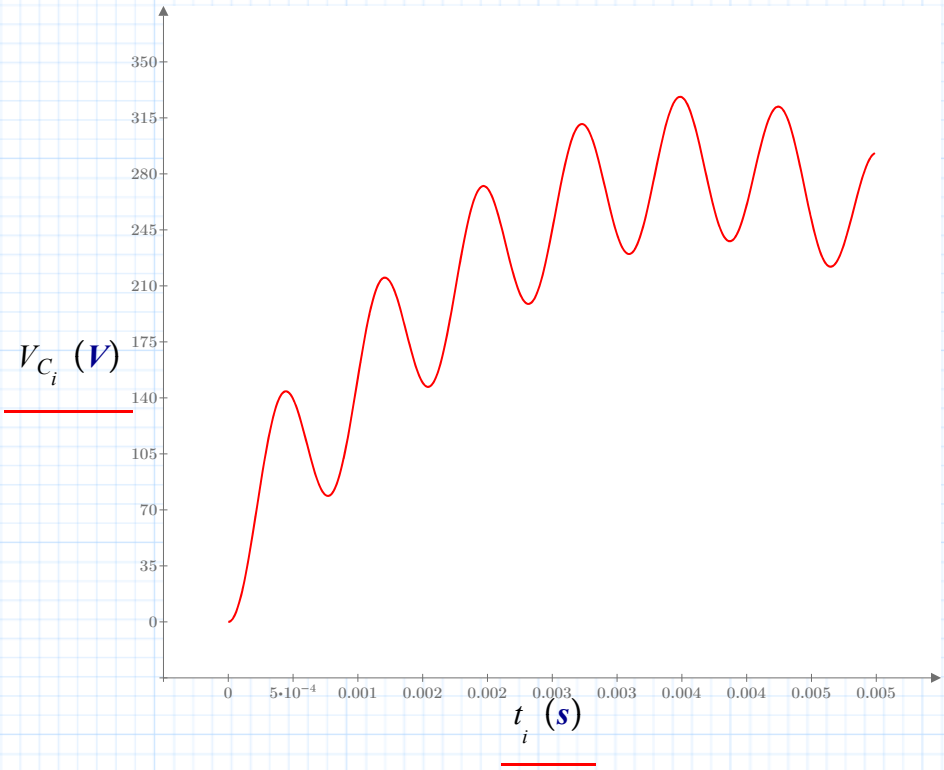

Fig. 3.1.5 Breaker recovery voltage